Configuring Resets Demo Script

Introduction

This demonstration provides high-level instructions on configuring the resets for the Zynq™ UltraScale+™ MPSoC.

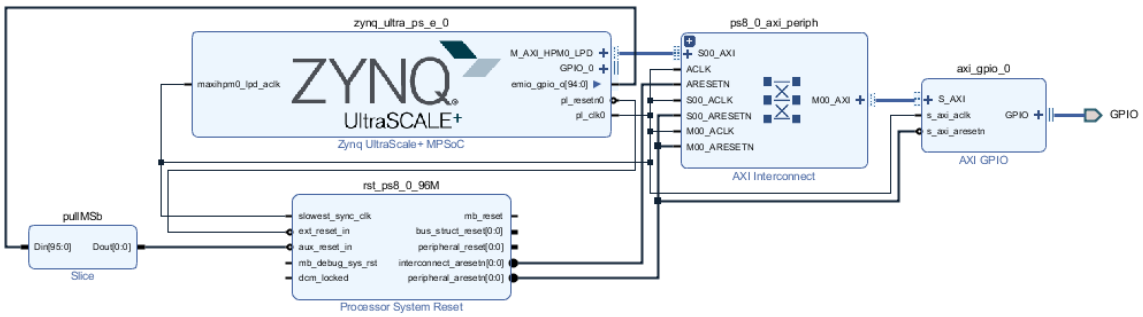
Preparation

- Necessary files are located at `$TRAINING_PATH/MPSoC_Resets/support` and `$TRAINING_PATH/CustEdIP`
  - `reset_demo_completer.tcl`
  - `completer_helper.tcl` (helper script containing common hardware operations)
- Required hardware: None
- Supporting materials:
  - Suggested: *Zynq UltraScale+ MPSoC Technical Reference Guide* (UG1085)

Configuring Clocks and Resets

Action with Description	Point of Emphasis and Key Takeaway
• Click the **Vivado** icon to launch the Vivado™ Design Suite.	

• From the Tcl command console:
`cd $::env(TRAINING_PATH)/MPSoC_Resets/support`
• Load the Tcl script provided to build the project:
`source reset_demo_completer.tcl`
• Specify the default language, platform, and processor:
`use VHDL`
`use ZCU104`
`use APU`
• Build the hardware:
`make buildStartingPoint`
	• Builds a simple project with a Zynq UltraScale+ MPSoC device.

Action with Description	Point of Emphasis and Key Takeaway
• Start by comparing the resets from the Zynq SoC PS to those available in the Zynq UltraScale+ MPSoC PS. • The Zynq SoC PS has a reset available to the PL for each of the four clock domains that it drives. • The Zynq UltraScale+ MPSoC PS offers no such resets.	
Now look at the rest of the provided design that was built when the demo was started. • The Tcl file generated a block design with GPIO connects to the LED on the ZCU104 board. The GPIO is connected to the clock and reset. • The block design should resemble the figure below.	
	
Question: Clocks and resets are usually coupled in some way. Why? Answer: Because the resets must be synchronous to a clock. Otherwise, there may be issues when an element enters or exits reset.	

Action with Description	Point of Emphasis and Key Takeaway
• Click the net connected to **pl_clk0** on the PS. • Notice the connections, especially to the Processor System Reset block.	• The importance here is that the clock is tied to the reset block and therefore the resets are synchronous to this clock.

Question: Where did the Processor System Reset block come from?

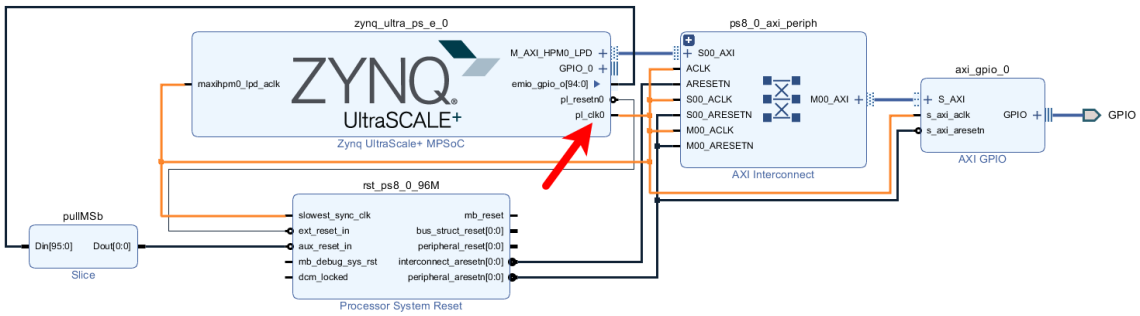
Answer: When the Run Connection Automation tool runs, it will automatically instantiate the Processor System Reset block to provide the necessary resets to an AXI-based system.

Question: What resets are available? When do you think they might be used?

Answer:

- mb_reset: For the MicroBlaze™ processor (if present).
- bus_struct_reset: Reset for certain types of buses.
- peripheral_reset: Active high reset.
- interconnect_aresetn: Used to reset the interconnect. The interconnect must come out of reset earlier than the peripherals.
- peripheral_aresetn: Active low reset for the peripherals.

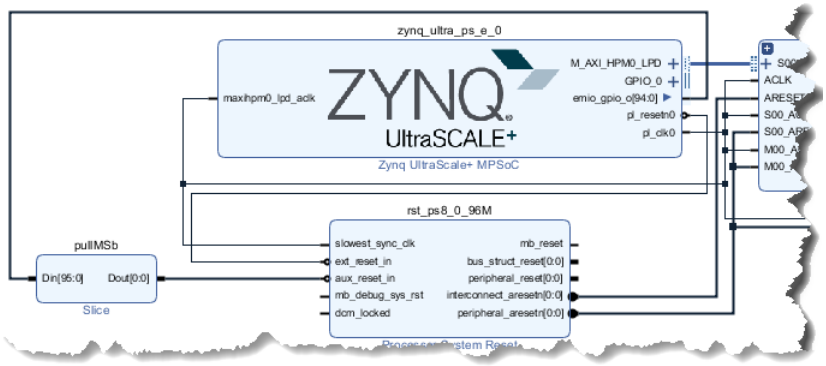
Clock line:



Question: So how can the user cause the logic in the PL to reset?

Answer: Use the EMIO GPIO.

Now look at another portion of the design.

Action with Description	Point of Emphasis and Key Takeaway
• Expand the PS's GPIO_O interface to reveal emio_gpio_0[94:0].	• Unlike the PS in the Zynq-7000 SoC, which only has 64 GPIO signals connecting the PS to the PL, the Zynq UltraScale MPSoC offers 95 connections.
• Knowing that the EMIO GPIO can be used and that only one signal is needed to indicate a reset to the PL, a slice is used to extract one of the 96 signals from the emio_gpio_o bus.	
	
• The one-bit wide signal is fed from the slice into the external reset pin of the Processor System Reset block. • It could have been fed into ext_reset_in just as easily if an aux_reset_in were required. • Remember that this is an active low input, so the software would have to drive this signal high to bring the logic in the PL out of reset. You could just as easily add an inverter between the slice and Processor System Reset block to have this be an active high reset.	
• Close the Vivado Design Suite.	

Summary

This demo showed one way to configure the primary reset from the Zynq UltraScale+ MPSoC PS to the PL. As you have seen, not all resets are controlled by the dedicated silicon. Users can create their own as needed.